REMARKS

This Amendment is responsive to the Office Action of March 17, 2004. Claims 1 – 20 are pending in this application. Reexamination and reconsideration are respectfully requested.

Preliminarily, the office action included a notice of informality due to the failure to list a separate post office address for the inventors in the declaration. However, the separate provision of a post office address is only required when it is different than the residence address. See 37 CFR section 1.63(c)(1). Accordingly, it is respectfully submitted the declaration as filed is in compliance with 37 CFR section 1.63(c)(1) and a substitute declaration is not required.

The Examiner rejected Claims 1, 2, 4, 5, 10, 11, 12, 15 – 17 and 20 under 35 USC 102(b) as being anticipated by Funada et al. This rejection is respectfully traversed.

The present invention as set out in independent claim 1 is directed to an amplifier employing an amplifier device having a nonlinear gain characteristic in the small signal region. For example, such an amplifier device may correspond to an LDMOS power transistor biased in a lower class AB or class B bias class. The present invention further provides a small signal linearization circuit for compensating for the small signal nonlinearity of the amplifier device. The provision of the small signal linearization circuit runs counter to conventional teachings of the power amplifier art which focus on the large signal region of the input signal which corresponds to the typical nonlinear operation region of the power amplifier. Applicants have determined that in power amplifiers employing certain types of amplifier devices (such as LDMOS devices) the

small signal region is actually an unrecognized source of nonlinearity. The small signal linearization circuit of the present invention provides for compensation of this nonlinearity (as set out in claim 1). The other independent claims (10 and 16) are directed to a feed forward amplifier and a method for compensating for nonlinearity in an amplifier, respectively, and equally provide for the correction of small signal nonlinearity in an amplifier device.

The Funada et al reference is directed to a feed forward amplifier which employs a generally conventional feed forward architecture employing a vector adjuster and pre-distortor in the main amplifier path. As shown in Fig. 1 and as stated, e.g. at Column 13, line 51- 53: "The distortion-detecting loop is equipped with a distributor 1, a vector adjuster 2, the pre-distortor 3, the main amplifier 4, a delay line 5, and a directional coupler 6." This is a conventional carrier cancellation loop in a feed forward architecture. In applying the Funada et al reference the Examiner indicated that the vector adjuster 2 and pre-distortor 3 corresponded to the small signal linearization circuit of the present invention. It is respectfully submitted, however, that this is an incorrect interpretation of the Funada et al reference. In fact when examined carefully it will be appreciated that the Funada et al reference not only fails to disclose a small signal linearization circuit but actually teaches directly away from the present invention and follows conventional teachings of the power amplifier art.

More specifically, in Funada et al the vector adjuster 2 comprises a gain adjuster (variable attenuator) and phase adjuster used in a conventional manner to minimize average power of the error signal to align the carrier cancellation loop (this circuitry generally corresponds to the conventional gain and phase control circuitry employed in input circuitry 20 in the present application; see specification page 9, lines 6 – 7). The

pre-distorter 3 of Funada et al in turn is adapted to predistort the input signal in a peak signal region to compensate for distortion introduced by the amplifier in this region. This is clearly shown in Fig. 2 of the Funada et al reference which shows pre-distortor correction only for the signal peak regions of the input signal to the pre-distortor 3. (See discussion in Column 14, line 60-67 and Column 15, line 1-16). More specifically, in FIG. 2(b), there is illustrated by the symbol T1 an example of the relationship between the level (the input level) of a signal that is input to the pre-distortor 3 and the level (the output level) of a signal that is output from the pre-distortor 3. Here, the abscissa axis represents the input level and the ordinate axis represents the output level. This graph of T1 clearly shows the operation of the pre-distortor 3 only in the large signal region of the input signal. Similarly Fig. 2(c) shows the operation of the pre-distortor 3 on the phase of the input signal only in the large signal region of the input signal (correction signal S1).

Therefore, Funada et al clearly does not disclose a "small signal linearization circuit". Also, the teachings of the Funada et al reference are consistent with the conventional teachings that only the large peak signal region is relevant for correction of nonlinearity effects and such teachings are directly away from the present invention. Equally distinguishing limitations are present in the other independent claims as will be appreciated by review of those claims and the above discussion of the Funada et al reference. Accordingly, it is respectfully submitted this rejection is fully traversed.

The Examiner rejected Claims 3, 6, 12, 14, 18 and 19 under 35 USC 103(a) as being unpatentable over Funada et al (Fig. 1). This rejection is respectfully traversed.

The above discussion of the rejection of the independent claims equally applies to the 103 rejection of these dependent claims. Accordingly, it is respectfully submitted this rejection is also fully traversed.

An IDS is attached hereto with an additional citation which was cited in a PCT search report in a corresponding International application. It is respectfully submitted this citation also fails to disclose or suggest the present invention.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance and a Notice of Allowance is respectfully requested. It is requested that the Examiner telephone the undersigned attorney if it appears that any impediment remains to allowance of the application.

Respectfully submitted,

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